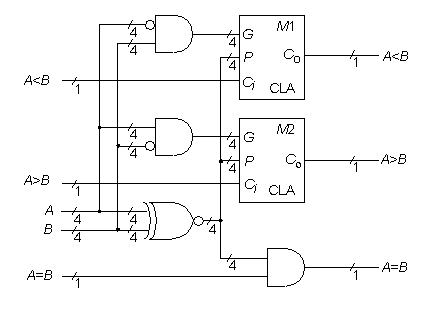
**74L85 4-Bit Magnitude Comparator**



**Statistics:** 11 inputs; 3 outputs; 33 gates;

**Function:** The 74L85 magnitude comparator can be functionally modeled as above. This is a simplification of implementing a magnitude comparator by a carry function with an inverted input bus as shown [here](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85generic.html). Using this concept, common elements of the three comparator functions A < B, A > B, and A = B are combined to construct the model shown above, which maps directly onto the gate-level realization of the 74L85.

**Models:**

* [74L85 ISCAS-85 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85.isc)
* [74L85 Verilog structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85.v)
* [74L85 behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85b.v)
* [74L85 complete gate-level tests (A<B, A>B, A=B, A[3:0], B[3:0])](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/74L85.tests)

**Generic Magnitude Comparator**

